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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/652,495
Filing Date	August 31, 2000
First Named Inventor	Salman Akram
Group Art Unit	2811
Examiner Name	N. Parekh
Attorney Docket Number	2269-3847US (98-0541.00/US)

ENCLOSURES *(check all that apply)*

- ☒ Postcard receipt acknowledgment (attached to the front of this transmittal)
- ☒ Duplicate copy of this transmittal sheet in the event that additional filing fees are required under 37 C.F.R. § 1.16
- ☐ Preliminary Amendment
- ☐ Response to Restriction Requirement/Election of Species Requirement dated
- ☐ Amendment in response to office action dated
- ☐ Amendment under 37 C.F.R. § 1.116 in response to final office action dated
- ☐ Additional claims fee - Check No. in the amount of $
- ☐ Letter to Chief Draftsman and copy of FIGS. with changes made in red
- ☐ Transmittal of Formal Drawings
- ☐ Formal Drawings (sheets)
- ☐ Information Disclosure Statement, PTO/SB/08A (08-00); ☐ copy of cited references
- ☐ Supplemental Information Disclosure Statement; PTO/SB/08A (08-00); copy of cited references and Check No. in the amount of $180.00
- ☐ Associate Power of Attorney
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- ☐ Petition
- ☒ Appeal Brief (18 pages); Claims Appendix (9 pages); Check no. 8557 in the amount of $500.00
- ☐ Certified Copy of Priority Document(s)
- ☐ Assignment Papers *(for an Application)*
- ☐ Terminal Disclaimer
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- ☐ Other Enclosure(s) *(please identify below)*:

Remarks

The Commissioner is authorized to charge any additional fees required but not submitted with any document or request requiring fee payment under 37 C.F.R. §§ 1.16 and 1.17 to Deposit Account 20-1469 during pendency of this application.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm *or* Individual name	Brick G. Power Registration No. 38,581
Signature	Brick G. Power
Date	October 24, 2005

CERTIFICATE OF MAILING

Express Mail Label Number: EL994844847US

Date of Deposit: October 24, 2005

Person Making Deposit: Tim Palfreyman

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Salman Akram

Serial No.: 09/652,495

Filed: August 31, 2000

For: CARRIER FOR WAFER-SCALE PACKAGE, WAFER-SCALE PACKAGE INCLUDING THE CARRIER, AND METHODS

Confirmation No.: 3659

Examiner: N. Parekh

Group Art Unit: 2811

Attorney Docket No.: 2269-3847US

NOTICE OF EXPRESS MAILING

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APPEAL BRIEF

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Attn: Board of Patent Appeals and Interferences

Sirs:

This APPEAL BRIEF is being submitted in the format required by 37 C.F.R. § 41.37(c)(1), with the fee required by 37 C.F.R. § 41.20(b)(2).

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I. REAL PARTY IN INTEREST

U.S. Serial No. 09/652,495 (hereinafter "the '495 Application), the application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc. The assignment was recorded with the United States Patent & Trademark Office (hereinafter the "Office") on August 31, 2000, at Reel 011070, Frame 0823. Accordingly, Micron Technology, Inc. is the real party in interest to the above-referenced appeal.

II. RELATED APPEALS AND INTERFERENCES

Neither Appellant nor the undersigned attorney is aware of any appeals, interferences, or any other actions currently ongoing before the Board of Patent Appeals and Interferences (hereinafter "the Board") or any federal court that may affect or be affected by the decision of the Board on this appeal of the Examiner's final rejections of the claims of the '495 Application.

III. STATUS OF THE CLAIMS

Claims 1-3, 5-41, and 43-55 are currently pending and under consideration in the '495 Application. Each of these claims stands finally rejected. The final rejections of claims 1-3, 5-41, and 43-55 are being appealed.

IV. STATUS OF AMENDMENTS

The '495 Application was filed on August 31, 2000, with seventy-two (72) claims.

A Preliminary Amendment was filed on January 16, 2001.

On November 30, 2001, a Restriction Requirement was mailed by the Office. A response to the Restriction Requirement was mailed on December 11, 2001, in which an election was made, without traverse, to prosecute claims 1-55.

The U.S. Patent & Trademark Office (hereinafter "the Office") sent a first action on the merits of claims 1-55 on April 8, 2002. An Amendment was filed on July 8, 2002, in response to the first Office Action. In that Amendment, claims 4, 42, and 56-72 were canceled without prejudice or disclaimer and several other claim revisions were presented, as were remarks supporting Appellant's position that the claims were allowable over the art upon which the Examiner's rejections were based.

On October 11, 2002, a final action was mailed. The Examiner revised his prior grounds for rejecting the claims. An Amendment Under 37 C.F.R. § 1.116 was mailed on December 4, 2002. An Advisory Action followed on December 19, 2002. In order to ensure entry of the previously submitted claim amendments, a Request for Continued Examination (RCE) was filed on December 16, 2003.

A non-final action on the merits of claims 1-3, 5-41, and 43-55 followed the RCE on March 13, 2003. Again, the grounds for rejecting the claims had been changed. Since then, the Examiner has not altered his grounds for rejecting claims 1-3, 5-41, and 43-55. On June 13, 2003, a Response was mailed.

Another final Office Action followed on September 4, 2003. On November 4, 2003, another Amendment Under 37 C.F.R. § 1.116 was mailed. In an Advisory Action dated December 12, 2003, the Examiner refused to consider or enter the amendments that had been

presented in the Amendment Under 37 C.F.R. § 1.116. Therefore, on December 16, 2003, another RCE was filed.

The RCE of December 16, 2003, was followed by another non-final action, which was dated February 19, 2004. A Response to that Office Action was mailed on May 19, 2004.

In his continued refusal to seriously consider the remarks that had been presented in support of the patentability of claims 1-3, 5-41, and 43-55, the Examiner issued another Final Office Action on July 30, 2004. Another Amendment Under 37 C.F.R. § 1.116 was mailed on September 30, 2004.

The finality of the prior Office Action was withdrawn in an Office Action that was mailed on January 4, 2005. Nonetheless, all of the pending claims were still rejected. A response to the January 4, 2005, Office Action was submitted on April 4, 2005.

Another Final Office Action was sent on June 20, 2005. On August 8, 2005, a Response to the Final Office Action was mailed. The reasoning that was presented in the Response of August 8, 2005, was again rejected, as evidenced by the Advisory Action of August 22, 2005.

In view of the Examiner's continued refusal to recognize the differences between the claimed subject matter and that disclosed in the art that had been considered, as well as the lengthy prosecution of the above-referenced application, a Notice of Appeal was filed on August 23, 2005.

This APPEAL BRIEF follows the Notice of Appeal, is being filed by Monday, October 24, 2005, and, since October 23, 3005, falls on a Sunday, should be deemed to have been filed within two months of the date on which the Notice of Appeal was filed. 37 C.F.R. § 1.7.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Several of the claims that have been considered in the '495 Application are directed to chip-scale packages. Such a chip-scale package includes a semiconductor device and a substrate. *See, e.g.,* Fig. 7A. The substrate, which comprises a semiconductor material, has a surface that faces the semiconductor device and another, opposite surface that faces away from the semiconductor device. *See, e.g.,* Fig. 7A. At least one electrically conductive via extends through the substrate. *See, e.g.,* Fig. 7A; page 5, lines 17-21. The substrate also includes at least one conductive trace that communicates with the at least one electrically conductive via and is carried by the surface of the substrate that faces away from the semiconductor device. *See, e.g.,* Fig. 7A; page 7, lines 1-3.

Other claims are drawn to a carrier, or substrate, that includes at least one via and at least one conductive trace that extends from the via. *See, e.g.,* Fig. 7A; page 5, lines 17-21. The at least one via is located so as to align with a corresponding bond pad of a semiconductor device when a surface of the carrier is positioned against the active surface of the semiconductor device. The at least one conductive trace is carried by another, opposite surface of the carrier, which is to face away from a semiconductor device when the carrier is assembled with the semiconductor device. *See, e.g.,* Fig. 7A; page 7, lines 1-3.

VI. ISSUES

(A) Whether claims 1-3, 5-10, 15, 18, 19, 21, 22, 26- 28, 30- 36, 43, 44, and 50-52 recite subject matter that, under 35 U.S.C. § 103(a), is not obvious in view of, and thus is

patentable over, the subject matter taught in U.S. Patent 6,004,867 to Kim et al. (hereinafter "Kim"), in view of the teachings of U.S. Patent 5,258,648 to Lin (hereinafter "Lin");

(B) Whether, under 35 U.S.C. § 103(a), the subject matter recited in each of claims 11-14, 20, 23-25, 37-41, and 45-49 is allowable over teachings from Kim, in view of teachings from Lin and, further, in view of the subject matter taught in U.S. Patent 5,229,647 to Gnadinger (hereinafter "Gnadinger"); and

(C) Whether claims 16, 17, 29, and 53-55 recite subject matter that is patentable under 35 U.S.C. § 103(a) over teachings from Kim, in view of the teachings of Lin and, further, in view of the subject matter taught in U.S. Patent 6,294,405 to Higgins, III (hereinafter "Higgins").

VII. ARGUMENT

Each of claims 1-3, 5-41, and 43-55 has been rejected under 35 U.S.C. § 103(a).

1. RELEVANT LAW

The standard for establishing and upholding a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

2. REFERENCES RELIED UPON

Kim

The teachings of Kim are drawn to substrates that include conductive traces that are carried either internally within the substrate (col. 3, line 55) or on a surface that is to be disposed against a semiconductor die (FIGs. 1 and 2).

While Kim teaches that the conductive traces may be located anywhere *in* the substrate (col. 3, line 55) or at a surface of the substrate which is to be disposed against the semiconductor die (FIGs. 1 and 2), Kim does not teach or suggest that the conductive traces may be carried upon the opposite, exposed surface of the substrate. *See* Final Office Action, pages 3-4. Instead, the teachings of Kim are clearly limited to a substrate with conductive traces that are carried by the surface that is to be positioned against a semiconductor device. *See, e.g.,* FIGs. 1-3; 5C-5E; col. 3, lines 40-46.

Lin

Lin teaches a composite flip chip semiconductor device. Col. 1, lines 28-31. The semiconductor device of Lin lacks a conventional package body, minimizing the size thereof. Col. 1, lines 52-54. The semiconductor devices of Lin include interposers. Conductive traces are carried on the surfaces of the interposers that are to be positioned against the active surfaces of semiconductor dice. FIGs. 1 and 5. The surfaces of the interposers that face away from the semiconductor dice do not carry conductive traces; they merely carry terminals. *See id.* Solder balls 42 or so-called "terminal groupings" 43, 44 may be secured to and protrude from the

terminals of the interposers of Lin. Lin teaches that terminal groupings 43, 44, are like and "can be used in place of a plurality of solder balls to couple, for example POWER and GROUND outputs." Col. 7, lines 50-54; Fig. 6.

Higgins

Higgins teaches a sub-chip-scale package having a substrate electrically connected to a semiconductor device, but lacks any teaching or suggestion of conductive traces on a surface of the substrate that is opposite the semiconductor device.

Gnadinger

Gnadinger teaches wafers having vias extending completely therethrough. Gnadinger lacks any teaching or suggestion of substrates with conductive traces on the surfaces thereof that are to face away, or be located opposite, from a semiconductor device with which the substrates are to be assembled.

3. ANALYSIS

a. KIM AND LIN

Claims 1-3, 5-10, 15, 18, 19, 21, 22, 26- 28, 30- 36, 43, 44, and 50-52 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter that is purportedly unpatentable over the subject matter taught in Kim, in view of teachings from Lin.

While Kim teaches that the conductive traces may be located anywhere *in* a substrate (col. 3, line 55) or at a surface of the substrate which is to be disposed against a semiconductor

die (FIGs. 1 and 2), Kim does not teach or suggest that the conductive traces may be carried upon the opposite, exposed surface of the substrate. *See* Final Office Action, pages 3-4. Instead, the teachings of Kim are clearly limited to a substrate with conductive traces that are carried by the surface that is to be positioned against a semiconductor device. *See, e.g.,* FIGs. 1-3; 5C-5E; col. 3, lines 40-46.

Lin also lacks any teaching or suggestion that a second surface of an interposer thereof, which is to be located opposite a semiconductor die, may carry at least one conductive trace. The surface of an interposer of Lin that faces away from a semiconductor die only carries terminals.

It is respectfully submitted that there are several reasons that the teachings of Kim and Lin do not support a *prima facie* case of obviousness against any of claims 1-3, 5-10, 15, 18, 19, 21, 22, 26-28, 30-36, 43, 44, or 50-52.

Kim and Lin Do Not Teach or Suggest Each and Every Claim Element

First, it is respectfully submitted that Kim and Lin, taken either separately or together, do not teach or suggest each and every element of any of claims 1-3, 5-10, 15, 18, 19, 21, 22, 26-28, 30-36, 43, 44, or 50-52.

Independent claim 1 recites a chip-scale package which includes a semiconductor device and a substrate with a first surface disposed adjacent an active surface of the semiconductor device. At least one electrically conductive via extends at least partially through the substrate to communicate with a corresponding bond pad of the semiconductor device. The substrate also includes a second surface, which is opposite from the first surface, which carries at least one conductive trace, which communicates with the at least one conductive via.

In contrast to independent claim 1, Kim and Lin, considered either in combination or independently, lack any teaching or suggestion of a chip-scale package having an interposer that includes conductive traces that communicate with conductive vias and that are carried upon a surface which is opposite the surface adjacent to which a semiconductor device is positioned, which is also the surface that faces away from a semiconductor device when the interposer is assembled with the semiconductor device (*e.g.*, the second surface of the substrate recited in independent claim 1). Instead, the teachings of both Kim and Lin are limited to interposers with conductive traces that extend across the surfaces that are to be positioned against semiconductor devices (*e.g.*, the first surface of the substrate recited in independent claim 1).

The "terminal groupings" mentioned in Lin are not conductive traces; instead, they are solder balls or solder ball-like protrusions that are used to form multiple electrical connections.

As Kim and Lin do not teach or suggest each and every element of independent claim 1, a *prima facie* case of obviousness has not been established against independent claim 1. Therefore, under 35 U.S.C. § 103(a), the subject matter recited in independent claim 1 is allowable over the teachings of Kim and Lin.

Claims 2, 3, 5-10, 15, 18, and 19 are each allowable, among other reasons, for depending either directly or indirectly from independent claim 1, which is allowable.

Independent claim 21 is directed to a chip-scale package with a substrate that includes first and second surfaces and a semiconductor device invertedly disposed adjacent to the first surface of the substrate. The first surface of the substrate includes contact areas that correspond

to an arrangement of bond pads on the semiconductor device. An opposite, second surface of the substrate, which faces away from the semiconductor device, carries at least one conductive trace.

Again, Kim and Lin, taken either collectively or individually, do not teach or suggest a substrate which includes a first surface, adjacent to which a semiconductor device is secured, and an opposite, second surface that carries at least one conductive trace. The teachings of Kim and Lin are limited to interposers with internally extending conductive traces, as well as to interposers with conductive traces that extend across a surface that is to be positioned against a semiconductor device (*e.g.,* the first surface of the substrate recited in independent claim 21). Furthermore, while Lin teaches that one or more "terminal groupings" may be positioned adjacent to the opposite surface of an interposer, Lin does not teach or suggest that these "terminal groupings" are conductive traces; rather, Lin teaches that the "terminal groupings" are like solder balls.

Therefore, the teachings of Kim and Lin cannot be relied upon to establish a *prima facie* case of obviousness against independent claim 21. Therefore, under 35 U.S.C. § 103(a), the subject matter recited in independent claim 21 is allowable over the subject matter taught in Kim and Lin.

Each of claims 22, 26-28, and 30-36 is allowable, among other reasons, for depending either directly or indirectly from independent claim 21, which is allowable.

Independent claim 43 is directed to a carrier with at least one via that extends from a first surface of the carrier, adjacent to which a semiconductor device is to be positioned, to an

opposite, second surface of the carrier. At least one conductive trace, which extends laterally from an end of the via, is carried by the second surface of the carrier.

Neither Kim nor Lin, taken together or separately, teaches or suggests an interposer with a first surface that is to be positioned adjacent a semiconductor device and an opposite, second surface that carries at least one conductive trace. To repeat: Lin lacks any teaching or suggestion that the "terminal groupings" mentioned therein are conductive traces; instead, Lin teaches that the "terminal groupings" can be used in place of solder balls. Inasmuch as Kim and Lin teach interposers that include conductive traces extending across the surfaces thereof, the teachings of both of these references are limited to conductive traces that extend across the surface of an interposer that is to be positioned against a semiconductor device (*e.g.,* the first surface of the substrate recited in independent claim 43).

Therefore, a *prima facie* case of obviousness has not been set forth against independent claim 43. Therefore, under 35 U.S.C. § 103(a), the subject matter to which independent claim 43 is drawn is allowable over the teachings of Kim and Lin.

Claims 44 and 50-52 are each allowable, among other reasons, for depending either directly or indirectly from independent claim 43.

There Is No Motivation to Combine the Teachings of Kim and Lin in the Asserted Manner

Second, it is respectfully submitted that one of ordinary skill in the art wouldn't have been motivated to combine the teachings of Kim and Lin in such a way as to support a *prima facie* case of obviousness.

Specifically, neither Kim nor Lin teaches or suggests an interposer with conductive traces that are carried upon an exposed surface thereof (*i.e.,* by a surface that is to face away from a semiconductor device). Thus, neither of these references could provide one of ordinary skill in the art with any motivation to combine their teachings in a manner that would render obvious the subject matter recited in any of claims 1-3, 5-10, 15, 18, 19, 21, 22, 26-28, 30-36, 43, 44, or 50-52.

Moreover, neither Kim nor Lin, when viewed collectively or individually, would have provided one or ordinary skill in the art with any suggestion or motivation to place a conductive trace of the interposer from Lin on the surface of the substrate of Kim that faces away from the semiconductor device of Kim in order to arrive at the chip-scale package of amended independent claim 1. As stated in Kim "[t]he electrically conductive traces 122 can be freely patterned **in** the substrate 120." Col. 3, lines 16-17 (emphasis added). Kim further states, "after the substrate 320 is firmly attached to the wafer 300, a substrate-wafer-composite 390 is formed. The top surface of the substrate 320 is back-lapped so that the terminal pads 324 **in** the substrate 320 are exposed." Col. 6, lines 16-21 (emphasis added); *see also*, FIG. 5D. While Kim teaches that terminals may be exposed during the back-lapping process, Kim does not teach or suggest that the back-lapping process exposes conductive traces.

Further, the conductive traces of the substrate of Kim perform the function of routing the vias to other electrical connections; therefore, the addition of traces to the surface would increase the cost of manufacturing the devices, which is contrary to a stated object of Kim. *See*, col. 1, lines 49-51.

In view of the foregoing, it appears that the Examiner improperly relied upon the hindsight provided by the above-referenced application to provide some motivation to combine the teachings of Kim and Lin in the manner that has been asserted.

Without any suggestion or motivation to combine the teachings of Kim and Lin, a *prima facie* case of obviousness has not been established against any of claims 1-3, 5-10, 15, 18, 19, 21, 22, 26-28, 30-36, 43, 44, or 50-52.

There Is No Reasonable Expectation of Success

Third, since neither Kim nor Lin teaches or suggests an interposer with conductive traces that are carried by a surface that will not face a semiconductor device, one of ordinary skill in the art would have had no reason to expect that the teachings of these references could have been successfully combined in such a way as to come up with a semiconductor device that includes an interposer with conductive traces on a surface that faces away from a semiconductor device.

Therefore, a *prima facie* case of obviousness has not been established against any of claims 1-3, 5-10, 15, 18, 19, 21, 22, 26-28, 30-36, 43, 44, or 50-52.

Accordingly, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 1-3, 5-10, 15, 18, 19, 21, 22, 26-28, 30-36, 43, 44, or 50-52 be reversed and that each of these claims be allowed.

Kim, Lin, and Gnadinger

Claims 11-14, 20, 23-25, 37-41, and 45-49 have been rejected under 35 U.S.C. § 103(a) for being drawn to subject matter that is assertedly unpatentable over teachings from Kim, in view of teachings from Lin and, further, in view of the subject matter taught in Gnadinger.

Each of claims 11-14 and 20 is allowable, among other reasons, for depending either directly or indirectly from independent claim 1,which is allowable.

Claims 23-25 and 37-41 are each allowable, among other reasons, for depending either directly or indirectly from independent claim 21, which is allowable.

Claims 45-49 are each allowable, among other reasons, for depending either directly or indirectly from independent claim 43, which is allowable.

It is further submitted that a *prima facie* case of obviousness cannot be established with regard to any of claims 11-14, 20, 23-25, 37-41, or 45-49 since one of ordinary skill in the art wouldn't have been motivated to combine teachings from Gnadinger with the teachings of either Kim or Lin in the asserted manner.

Gnadinger, which teaches wafers having vias extending completely therethrough, like Kim and Lin, lacks any teaching or suggestion of substrates with conductive traces on the surfaces thereof that are to face away, or be located opposite, from a semiconductor device with which the substrates are to be assembled (*e.g.*, the second surfaces of the substrates recited in independent claims 1, 21, and 43).

Additionally, Gnadinger does not include any teaching or suggestion that would provide one of ordinary skill in the art with a reason to expect the combination of teachings from Kim, Lin, and Gnadinger to be successful.

Thus, a *prima facie* case of obviousness cannot be established for any of claims 11-14, 20, 23-25, 37-41, or 45-49 under 35 U.S.C. § 103(a).

Kim, Lin, and Higgins

Claims 16, 17, 29, and 53-55 have been rejected under 35 U.S.C. § 103(a) for being directed to subject matter that is allegedly unpatentable over teachings from Kim, in view of the subject matter taught in Lin and, further, in view of the teachings of U.S. Patent 6,294,405 to Higgins, III (hereinafter "Higgins").

Claims 16 and 17, 29, and 53-55 are each allowable, among other reasons, for depending from independent claims 1, 21, and 43, respectively, each of which is allowable.

Furthermore, Higgins teaches a sub-chip-scale package having a substrate electrically connected to a semiconductor device, but, like Kim and Lin, lacks any teaching or suggestion of conductive traces on a surface of the substrate that is opposite the semiconductor device (*e.g.,* the second surfaces of the substrates recited in independent claims 1, 21, and 43) and, thus, the resultant combination of Higgins with Kim and Lin does not remedy the aforementioned deficiencies of Kim and Lin as required to establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a).

Thus, a *prima facie* case of obviousness cannot be established against any of claims 16, 17, 29 or 53-55 under 35 U.S.C. § 103(a).

In view of the foregoing, reversal of the 35 U.S.C. § 103(a) rejections of claims 1-3, 5-41, and 43-55 is respectfully solicited.

VIII. CLAIMS APPENDIX

The current status of each claim that has been introduced into the '783 Application is set forth in CLAIMS APPENDIX to this Appeal Brief.

IX. EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132. Accordingly, no evidence appendix accompanies this Appeal Brief.

X. RELATED PROCEEDINGS APPENDIX

No decisions have been rendered by the Board or any court in a related application. Therefore, this Appeal Brief is not accompanied by a related proceedings appendix.

XI. CONCLUSION

It is respectfully submitted that:

(A) Claims 1-3, 5-10, 15, 18, 19, 21, 22, 26- 28, 30- 36, 43, 44, and 50-52 recite subject matter that, under 35 U.S.C. § 103(a), is not obvious in view of, and thus patentable over, the subject matter taught in Kim, in view of the teachings of Lin;

(B) Under 35 U.S.C. § 103(a), the subject matter recited in each of claims 11-14, 20, 23-25, 37-41, and 45-49 is allowable over teachings from Kim, in view of teachings from Lin and, further, in view of the subject matter taught in Gnadinger; and

(C) Claims 16, 17, 29, and 53-55 are directed to subject matter that is patentable under 35 U.S.C. § 103(a) over teachings from Kim, in view of the teachings of Lin and, further, in view of the subject matter taught in Higgins.

In view of the foregoing, it is respectfully requested that the Examiner's rejections of claims 1-3, 5-41, and 43-55 be reversed and that each of these claims be allowed.

Respectfully submitted,

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BGP/eg
Document in ProLaw

CLAIMS APPENDIX

1. A chip-scale package, comprising:

a semiconductor device including an active surface; and

a substrate comprising a semiconductor material and including a first surface disposed adjacent the active surface and including:

at least one electrically conductive via extending at least partially therethrough, positioned over the semiconductor device, and in communication with a corresponding bond pad of the semiconductor device; and

at least one conductive trace in communication with the at least one electrically conductive via and carried on a second surface of the substrate, opposite from the first surface of the substrate.

2. The chip-scale package of claim 1, further comprising an electrically conductive bump protruding from the substrate opposite the semiconductor device, in communication with the at least one electrically conductive via, and located at an opposite end of the at least one conductive trace from the at least one electrically conductive via.

3. The chip-scale package of claim 1, wherein the substrate comprises at least another electrically conductive via that extends substantially directly therethrough.

5. The chip-scale package of claim 1, wherein a substrate of the semiconductor device and the substrate comprising semiconductor material comprise the same type of semiconductor material.

6. The chip-scale package of claim 1, wherein a substrate of the semiconductor device and the substrate comprising semiconductor material comprise materials having substantially the same coefficients of thermal expansion.

7. The chip-scale package of claim 1, wherein a substrate of the semiconductor device comprises silicon.

8. The chip-scale package of claim 1, wherein the semiconductor material comprises silicon.

9. The chip-scale package of claim 1, wherein a first thickness of the semiconductor device and a second thickness of the substrate are substantially the same.

10. The chip-scale package of claim 1, wherein a first thickness of the semiconductor device is greater than a second thickness of the substrate.

11. The chip-scale package of claim 1, wherein the another surface of the substrate is at least partially coated with an insulative material.

12. The chip-scale package of claim 11, wherein the insulative material comprises a layer extending substantially over the surface.

13. The chip-scale package of claim 11, wherein the insulative material comprises an oxide.

14. The chip-scale package of claim 11, wherein the insulative material comprises silicon oxide.

15. The chip-scale package of claim 1, further comprising an intermediate layer disposed between the semiconductor device and the substrate.

16. The chip-scale package of claim 15, wherein the intermediate layer comprises an adhesive material.

17. The chip-scale package of claim 15, wherein the intermediate layer comprises polyimide.

18. The chip-scale package of claim 15, wherein the at least one electrically conductive via and the corresponding bond pad communicate through the intermediate layer.

19. The chip-scale package of claim 1, wherein conductive material of the at least one electrically conductive via is bonded to the corresponding bond pad.

20. The chip-scale package of claim 1, wherein a contact between the at least one electrically conductive via and the corresponding bond pad comprises a diffusion region comprising a bond pad material and a via material.

21. A chip-scale package, comprising:

a substrate comprising semiconductor material and including:

a first surface with contact areas arranged correspondingly to an arrangement of bond pads on an active surface of a semiconductor device of the chip-scale package;

conductive vias extending therethrough and corresponding to the contact areas; and

a second surface opposite the first surface and carrying at least one conductive trace extending laterally from a conductive via of the conductive vias; and

the semiconductor device invertedly disposed adjacent to the first surface of the substrate so that bond pads of the semiconductor device communicate with corresponding conductive vias of the substrate.

22. The chip-scale package of claim 21, wherein the bond pads contact the corresponding conductive vias.

23. The chip-scale package of claim 22, further comprising diffusion regions between the bond pads and the corresponding conductive vias.

24. The chip-scale package of claim 23, wherein each of the diffusion regions comprises a bond pad material and a via material.

25. The chip-scale package of claim 24, wherein the diffusion regions at least partially secure the semiconductor device to the substrate.

26. The chip-scale package of claim 21, further comprising an intermediate layer disposed between the substrate and the semiconductor device.

27. The chip-scale package of claim 26, wherein the bond pads and the corresponding vias contact each other through the intermediate layer.

28. The chip-scale package of claim 26, wherein the intermediate layer comprises a material which adheres the semiconductor device to the substrate.

29. The chip-scale package of claim 26, wherein the intermediate layer comprises a polyimide.

30. The chip-scale package of claim 21, further comprising at least one conductive bump in communication with at least one conductive via of the corresponding conductive vias, protruding from the substrate opposite from the semiconductor device, and located at an opposite end of the at least one conductive trace from the at least one conductive via.

31. The chip-scale package of claim 30, wherein the at least one conductive bump comprises solder.

32. The chip-scale package of claim 21, wherein the substrate comprising semiconductor material and a substrate of the semiconductor device comprise the same material.

33. The chip-scale package of claim 21, wherein the substrate comprises silicon.

34. The chip-scale package of claim 21, wherein a substrate of the semiconductor device comprises silicon.

35. The chip-scale package of claim 21, wherein a first thickness of the substrate and a second thickness of the semiconductor device are substantially equal.

36. The chip-scale package of claim 21, wherein a first thickness of the substrate is less than a second thickness of the semiconductor device.

37. The chip-scale package of claim 21, further comprising an insulative material disposed on at least a portion of the second surface of the substrate.

38. The chip-scale package of claim 37, wherein at least one conductive via of the corresponding conductive vias is exposed through the insulative material.

39. The chip-scale package of claim 37, wherein the insulative material comprises an oxide.

40. The chip-scale package of claim 37, wherein the insulative material comprises silicon oxide.

41. The chip-scale package of claim 37, wherein the insulative material comprises an insulative layer disposed substantially over the second surface.

43. A flip-chip carrier, comprising a substrate comprising semiconductor material and including:

at least one via formed therethrough and having a first end located proximate a first surface of the substrate and positioned to substantially align with a corresponding bond pad of a semiconductor device to be positioned adjacent to the first surface of the substrate; and

at least one conductive trace laterally extending from a second end of the at least one via and carried by a second surface of the substrate, which is located opposite the first surface of the substrate.

44. The flip-chip carrier of claim 43, wherein the at least one via comprises an electrically conductive material.

45. The flip-chip carrier of claim 43, further comprising an insulative material disposed on at least a portion of at least one surface of the substrate.

46. The flip-chip carrier of claim 45, wherein the insulative material comprises an oxide.

47. The flip-chip carrier of claim 45, wherein the insulative material comprises silicon oxide.

48. The flip-chip carrier of claim 45, wherein the insulative material comprises an insulative layer disposed substantially over the at least one surface.

49. The flip-chip carrier of claim 45, wherein the at least one via is exposed through the insulative material.

50. The flip-chip carrier of claim 43, wherein the substrate comprises silicon.

51. The flip-chip carrier of claim 43, further comprising a conductive bump disposed adjacent an end of the at least one conductive trace located opposite from the second end of the at least one via.

52. The flip-chip carrier of claim 51, wherein the conductive bump comprises solder.

53. The flip-chip carrier of claim 43, further comprising an adhesive layer disposed adjacent the first surface of the substrate.

54. The flip-chip carrier of claim 53, wherein the adhesive layer comprises a polyimide.

55. The flip-chip carrier of claim 53, wherein the first end of the at least one via extends through the adhesive layer.